(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 December 2001 (27.12.2001)

PCT

(10) International Publication Number
WO 01/99184 A2

(51) International Patent Classification[7]: H01L 21/768

(21) International Application Number: PCT/US01/19881

(22) International Filing Date: 21 June 2001 (21.06.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/598,780 21 June 2000 (21.06.2000) US

(71) Applicant: INFINEON TECHNOLOGIES NORTH AMERICA CORP. [US/US]; 1730 North First Street, San Jose, CA 95112-4508 (US).

(72) Inventors: STETTER, Michael; 12-7 Loudon Dr., Fishkill, NY 12524 (US). KALTALIOGLU, Erdem; 16F Winthrop Road, Wappingers Falls, NY 12590 (US). COWLEY, Andy; 8 Summerlin Court, Wappingers Falls, NY 12590 (US).

(74) Agents: BRADEN, Stanton, C. et al.; Siemens Corporation - Intellectual Property Dept., 186 Wood Ave. South, Iselin, NJ 08830 (US).

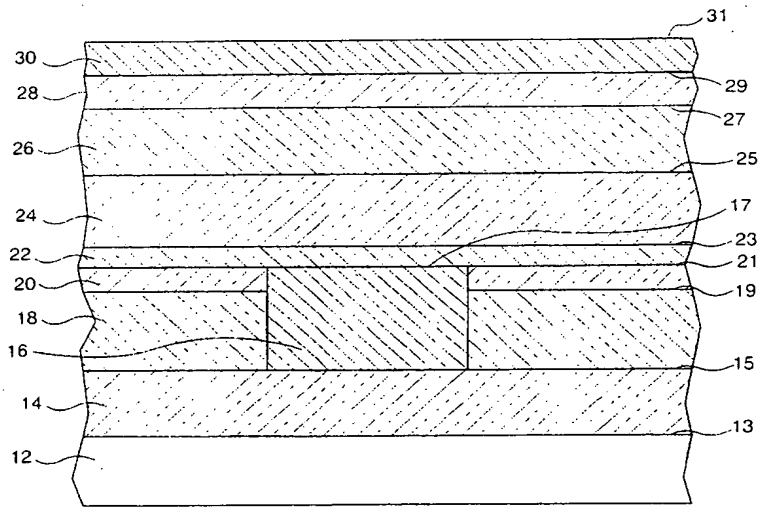
(81) Designated States *(national)*: JP, KR.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: DUAL DAMASCENE PROCESS UTILIZING A LOW-K DUAL DIELECTRIC



(57) Abstract: A method of fabricating an integrated circuit with a dual dielectric structure and utilizes a dual damascene process to fabricate metal interconnection layers. The dual dielectric structure consists of a first insulating layer of conventional dielectric material, and a second insulating layer of a second dielectric material with a low dielectric constant (low-k dielectric material). The first dielectric material is used in regions of the integrated circuit where the superior mechanical properties of conventional dielectric materials will result in maintaining the reliability and mechanical properties of the integrated circuit. The second dielectric material is used in regions of the integrated circuit where the low dielectric constant will result in improved speed of the integrated circuit and reduced electrical coupling between conductors in the integrated circuit. The fabrication of the dual dielectric structure is integrated with a dual damascene metallization process.

WO 01/99184 A2

DUAL DAMASCENE PROCESS UTILIZING A LOW-K DUAL DIELECTRIC

Field of the Invention

This invention relates to integrated circuits manufactured using multiple levels of conductive interconnection which make use of dielectric (or insulating) materials fabricated to provide a low value of dielectric constant, and more particularly, to structures fabricated using a dual damascene process to fabricate the multilevel interconnection.

Background of the Invention

Since the original invention of the integrated circuit the performance and density of such integrated circuits has increased by multiple orders of magnitude. These increases have resulted from many factors, including new and improved equipment for the fabrication of the integrated circuits, and the introduction into the structure of the integrated circuits of new, more complex, materials. As the density of the integrated circuits has increased due to the improved ability to fabricate finer and finer features, the factors which limit the performance (speed) of the circuits has changed. In particular, as the width and thickness of metal conductors, and the lateral spacing between conductors, has decreased, the resistance per unit length of the conductors has increased. Similarly, as the thickness of the insulating (dielectric) layers has decreased, the capacitance per unit area between various conductors has increased. The result has been that the factors limiting the speed performance of the integrated

circuits have more and more become the resistivity of the material forming the metal conductors and the dielectric constant of the insulating material surrounding the conductors.

The first factor, the resistivity of the material forming the metal conductors, has been addressed by a change from the predominant use of aluminum to the use of copper for the conductor material.

The second factor, the dielectric constant of the insulating layers in the structure, has been addressed by the increasing use of insulting materials with a lower dielectric constant (or low-k materials or dielectrics) than the commonly used silicon dioxide or silicon nitride. Two general approaches to the use of lower dielectric constant materials are presently in evaluation or limited use in commercially available products. One of these is the use of organic materials to replace the inorganic silicon oxide or silicon nitride. The second approach is the use of inorganic materials containing voids or bubbles.

Both of these approaches to having a low-k dielectric suffer from some inherent weaknesses and drawbacks. One of these is that the materials generally have less desirable mechanical properties than the traditional materials they are replacing. The low-k dielectric materials presently available have been found to be relatively soft (lower moduli of elasticity), to have lower tensile and compressive strength, to have lower thermal conductivity, and to have a higher

coefficient of thermal expansion, than the materials they are designed to replace.

The lower moduli of elasticity and lower tensile and compressive strength lead to structures which are mechanically unstable, which move and crack when subjected to temperature cycling, and which are subject to damage when subjected to the mechanical forces involved in operations such as wire bonding.

When the temperature of an integrated circuit rises during operation or because of a rise in ambient temperature, the higher coefficient of thermal expansion of the low-k dielectric material leads to the situation where the metal vias interconnecting different levels of conductors come under tensile stress. This will tend to pull apart conductors in vias of the integrated circuit which can result in intermittent or failed interconnections and lead to lower reliability of the integrated circuits. In the conventional structures the conductors in vias are under compressive stress when the temperature of the integrated circuit rises.

Further, the available methods for etching via openings through the dielectric materials make use of some specific properties of the commonly used silicon oxide dielectric to achieve the required control of the via etching process. Specifically, the by-products resulting from commonly used silicon oxide etching processes deposit on sidewalls of etched portions of vias, and passivate sidewalls thereof and protect them from additional etching. When the etch process is completed, these passivating by-products can be removed using

a simple ashing process, wherein the passivating material is oxidized to a powdery substance and can then be removed in a cleaning operation.

There is a need to provide a structure, and a method for fabricating said structure, which allows the designers of integrated circuits to take advantage of the desirable low dielectric constant of the low-k materials, while simultaneously alleviating the effects of the undesirable mechanical properties of these materials.

Summary of the Invention

The present invention is directed to an integrated circuit structure, and a method for fabricating an integrated circuit structure using a dual damascene metallization process, which allows for the use of conventional silicon dioxide dielectric material in the regions of the structure where the superior mechanical and chemical properties of the silicon dioxide can be used advantageously, and which allows for the use of low-k dielectric materials in the regions of the structure where the lower dielectric constant can be advantageously used to provide circuits which operate at higher speeds, and where the poorer mechanical properties of the low-k dielectric material do not cause a degradation in the mechanical properties or reliability of the integrated circuit.

Specifically, conventional silicon oxide dielectric is used in the vicinity of the via structures which interconnect different levels of metallization, and where the structure may

be subjected to high mechanical stress such as the regions of the bonding pads. The low-k dielectric material is used in the remaining regions of the integrated circuit where the low dielectric constant results in reduced capacitance between conductors and ground and between individual conductors, with a resulting reduction in coupling between conductors.

The present invention is integrated into a commonly used process sequence usually denoted as a "dual damascene" process. A damascene process sequence is a method used to define a level of conductive interconnect wherein the conductive metal lines are defined not by patterning and etching the metal conductor, but rather by defining trenches in an insulating layer, and a metal conductor is then deposited into these trenches. The width of the metal conductor is determined by the width of the trenches which have been defined in the dielectric material. This method of defining metal conductor patterns has an advantage over the more traditional methods in that dielectric materials can be more easily and precisely etched than can typical metal conductors used in integrated circuit fabrication. In the dual damascene process, after the trenches (into which metal conductor will subsequently be deposited) have been patterned and etched, via holes are patterned in the interior regions of the previously defined trenches. These via holes are then etched through to the underlying interconnect layers or circuit elements. The via holes and trenches are then filled with the interconnect metal.

Viewed from a method aspect, the present invention is directed to a method for fabricating an integrated circuit using a dual damascene process to form an interconnect level over a top surface of a semiconductor body in which an insulator underlying a metal conductor of the interconnect level and extending laterally beyond the conductor is of a first dielectric material having a first dielectric constant, and an insulator lying to the sides of the metal conductor is of a second dielectric material having a second dielectric constant which is different than the first dielectric constant. The method comprises the steps of: depositing over a semiconductor body, upon which it is desired to form an interconnect level, a first insulating layer of the first dielectric material, and further depositing a second insulating layer of the second dielectric material over the first insulating layer; depositing over the second insulating layer of second dielectric material a first masking layer of a first masking material, and a second masking layer of a second masking material, where the first and second masking materials are chosen so as to be mutually selective to each other in their etching characteristics, such that at least one etchant which etches the first masking material will not etch the second masking material, and at least one etchant which etches the second masking material will not etch the first masking material; defining and etching in the second masking layer an opening which will ultimately define the location and features of a metal conductor, etching said second masking material

with an etchant which will not etch said first masking material; defining and etching in the first masking layer an opening which will ultimately define the location and size of a via opening to underlying metal conductors or circuit elements, etching said first masking material with an etchant which will not etch said second masking material; using the first and second masking layers as an etch mask, continuing the etching process of the via opening through the second insulating layer, etching said second dielectric material with an etchant which will not etch the first masking material, and stopping the etch at the top surface of the first insulating layer; using the second insulating layer as a mask, etching through the first insulating layer to extend the via opening, stopping at a surface of the semiconductor body, simultaneously etching the exposed portion of the first masking layer; using the first and second masking layers as a mask, etching the second insulating layer through to the surface of the first insulating layer, simultaneously etching any exposed portion of any protective cap layer on the surface of the semiconductor body, and exposing the top surface of a metal conductor or circuit element at the bottom of the via opening; depositing upon the semiconductor body a layer of metal conductor such as to contact the top surface of any underlying metal conductor or circuit element, to fill the previously opened via opening, to fill the previously defined opening in the second insulating layer, and overfilling said opening above the level of the top surface of the second

masking level; and planarizing the top surface of the semiconductor body so as to remove all metal conductor material above the top surface of the first masking layer and to remove the second masking layer.

The present invention will be better understood from the following more detailed description taken with the accompanying drawings and claims.

Brief Description of the Drawing

FIG. 1 shows a sectional view of an integrated circuit structure fabricated using the methods of the present invention; and

FIGS. 2-7 show the integrated circuit structure at various points throughout the fabrication process.

The drawings are not necessarily to scale.

Detailed Description

FIG. 1 shows a schematic sectional view of an integrated circuit structure 10 in accordance with an exemplary embodiment of the present invention. The structure 10 comprises a semiconductor body 12 having a top surface 13. Transistors and other devices (not shown) fabricated in and/or on semiconductor body 12 would be connected to elements of an interconnect structure using conventional techniques. An insulating layer 14 having a top surface 15 is formed on the top surface 13 of semiconductor body 12. A conductor 16 having a top surface 17 and an insulating layer 18 having a top surface 19 are formed on the top surface 15 of the insulating layer 14. Although not shown, layer 16 selectively

can pass through layer 14 and contact portions of body 12 and/or diffusions (not shown) therein. Insulating layer 18 is capped with a hard mask layer 20 having a top surface 21. Conductor 16, insulating layer 18, and hard mask 20 could be formed using conventional metal etching processes, a conventional damascene process, a conventional dual damascene process, or by using the novel process of the present invention which is discussed below. The conductor 16 and hard mask 20 are covered by cap layer 22 having a top surface 23. A conductor 36, comprising portions 36a and 36aa, has portion 36aa in contact with conductor 16 and portion 36a. A dashed line 36aaa delineates between the two portions 36a and 36aa of conductor 36. Conductor portion 36a serves as an interconnection between various parts of the integrated circuit. Conductor portion 36a has a top surface 36t, a bottom surface 36b, and side surfaces 36c. Conductor portion 36aa has side surfaces 36s. An insulating layer 24 has a top surface 25 and surrounds conductor portion 36aa and lies underneath a bottom surface 36b of conductor portion 36a, extending out to cover a top surface 23 of cap layer 22. An insulating layer 26 has a top surface 27 and lies adjacent to side surfaces 36c of conductor portion 36a. A cap layer 28 has a top surface 29 and covers the top surface 27 of insulating layer 26.

A method in accordance with the present invention for fabricating the structure 10 shown in FIG. 1 is described herein below.

FIG. 2 shows a sectional view of the integrated circuit structure 10 at an early stage of fabrication. Fabrication has progressed to the point in the process sequence where a first level of metal conductor 16 having a top surface 17 has been defined on a top surface 15 of an insulating layer 14 which has been fabricated on a top surface 13 of a semiconductor body 12. Transistors which have been fabricated in the semiconductor body 12 are not shown, but would be connected to elements of the interconnect structure using conventional techniques. The conductor 16 is surrounded by dielectric material 18 having a top surface 19, which is capped by a hard mask layer 20 having a top surface 21. Conductor 16, insulating layer 18, and hard mask 20 could be formed using conventional metal etching processes, a conventional damascene process, a conventional dual damascene process, or by using the novel process of the present invention. The metal 16 and hard mask 20 are covered by a cap layer 22 having a top surface 23. The insulating layers 14 and 18 might consist of a conventional dielectric such as silicon dioxide, a low-k dielectric material, or a composite dielectric composed of conventional and low-k dielectric material, as are described herein

FIG. 3 shows the integrated circuit structure 10 after the first steps in the process to fabricate a second conductor layer using a dual damascene process and using a combination of conventional and low-k dielectric materials. The steps which have been completed include the deposition of a

conventional silicon oxide insulating layer 24 having a top surface 25, the deposition of a low dielectric constant (low-k) insulating layer 26 having a top surface 27, and the deposition of a dual hard mask layer consisting of layers 28 and 30 having top surfaces 29 and 31, respectively. Layer 28 forms a cap layer for the low-k dielectric layer 26 and consists of a material, such as silicon nitride, which is compatible with the underlying low-k dielectric material of layer 26. Layer 30 forms a hard mask layer on top of layer 28, and typically would be a metallic material such as tungsten. The major requirement on the two layers 28 and 30 is that they be mutually selective to each other in their etching characteristics, that is, etchants which etch the material of layer 30 do not etch the material of layer 28 at any significant rate, and etchants which etch the material of layer 28 do not etch the material of layer 30 at any significant rate.

FIG. 4 shows the integrated circuit structure 10 after an opening 32 has been defined and etched in the hard mask layer 30. The opening 32 will subsequently be filled with metal conductor to form the conductor 36a shown in FIG. 1. The etchant used to etch the material of layer 30 has not etched any significant amount of the material of layer 28, and the etch process has stopped at or near the top surface 29 of layer 28. Conventional photolithographic techniques are used to define an opening in a photoresist material (not shown),

and the photoresist material has subsequently been removed after the completion of the etch process.

FIG. 5 shows the integrated circuit structure 10 after an opening 34 has been defined and etched, using a suitable etchant material, through the cap layer 28 and down through the low-k insulating layer 26, stopping at the top surface 25 of the conventional insulating layer 24. The area below opening 34 is to be a via which will be filled with metal. Conventional photolithographic techniques are used to define an opening in a photoresist material (not shown), the photoresist material is used to define the opening etched in the cap layer 28, and the photoresist material has subsequently been removed after the completion of the etch processes. The etchant used to etch the low-k insulating layer 26 is chosen to be selective so as not to etch the material of cap layer 28 nor conventional insulating layer 24.

FIG. 6 shows the integrated circuit structure 10 after an etch process has been completed to extend the depth of the opening 34 through the conventional insulating layer 24 down to the top surface 23 of the cap layer 22. The extended opening 34 is identified as 34a. The etchant is chosen so as to selectively etch the material of insulating layer 24 and also to etch the material of cap layer 28 so as to extend the opening 32 down to the top surface 27 of low-k insulating layer 26, while not etching the material of the cap layer 22 or the low-k insulating layer 26, to result in an opening 32a.

FIG. 7 shows the integrated circuit structure 10 after an etch process has been completed to extend opening 32a through the low-k insulating layer 26 down to the top surface 25 of conventional insulating layer 24 to form opening 32aa. An additional etch is performed to remove the cap layer 22 at the bottom of the opening 34a to result in opening 34aa. The top surface 17 of the metal layer 16 is exposed at the bottom of extended opening 34aa.

FIG. 1 shows the integrated circuit structure 10 after the structure of FIG. 7 has been subjected to a conventional dual damascene process consisting of a standard metal liner fill, deposition of a seed layer, and metal plating, followed by a chemical mechanical polishing (CMP) to planarize the surface of the integrated circuit structure 10. The hard mask layer 30 is removed by the CMP process. The structure illustrates the opening 34aa filled with metal to form the conductor 36aa, and the opening 32aa filled with metal to form the conductor 36a.

As shown in FIG. 1, the dielectric portion of the region of the integrated circuit structure 10 in the vicinity of via 34aa, filled with metal 36aa and lying between metal conductor 16 and metal conductor 36a, is composed of conventional dielectric material 24. The portion of the integrated circuit 10 to either side 36c of metal conductor 36aa is composed of the low-k dielectric material 26.

It can be readily appreciated that the specific embodiment described is merely illustrative of the basic

principles of the invention and that various other embodiments may be devised without departing from the spirit and novel principles of the invention. Further, it can be readily appreciated that the specific process steps and sequence of said process steps is merely illustrative of the basic principles of the invention, and that various other process steps may be devised, and the sequence of said process steps may be modified, without departing from the spirit and novel principles of the present invention. For example, various etch processes which are described as being performed in one process step may be separated into a sequence of separate process steps, and similarly, various etch processes which are described as being performed in a sequence of separate process steps may be performed in one single integrated process step. Further, various materials and classes of materials may be substituted for the materials specified in the various masking and insulating layers. Furthermore, while the structure and method for fabricating said structure are described in the context of fabricating a silicon integrated circuit, the method may be applied to fabricating similar structures in various devices and circuits fabricated using semiconducting materials other than silicon, and may also be applied to the fabrication of passive interconnection structures such as printed wiring boards, flexible interconnection circuits, and integrated circuit package structures.

What is claimed is:

1. A method for fabricating an integrated circuit using a dual damascene process to form an interconnect level over a top surface of a semiconductor body in which an insulator underlying a metal conductor of the interconnect level and extending laterally beyond the conductor is of a first dielectric material having a first dielectric constant, and an insulator lying to the sides of the metal conductor is of a second dielectric material having a second dielectric constant which is different than the first dielectric constant, said method comprising the steps of:

depositing over a semiconductor body, upon which it is desired to form an interconnect level, a first insulating layer of the first dielectric material, and further depositing a second insulating layer of the second dielectric material over the first insulating layer;

depositing over the second insulating layer of second dielectric material a first masking layer of a first masking material, and a second masking layer of a second masking material, where the first and second masking materials are chosen so as to be mutually selective to each other in their etching characteristics, such that at least one etchant which etches the first masking material will not etch the second masking material, and at least one etchant which etches the second masking material will not etch the first masking material;

defining and etching in the second masking layer an opening which will ultimately define the location and features of a metal conductor, etching said second masking material with an etchant which will not etch said first masking material;

defining and etching in the first masking layer an opening which will ultimately define the location and size of a via opening to underlying metal conductors or circuit elements, etching said first masking material with an etchant which will not etch said second masking material;

using the first and second masking layers as an etch mask, continuing the etching process of the via opening through the second insulating layer, etching said second dielectric material with an etchant which will not etch the first masking material, and stopping the etch at the top surface of the first insulating layer;

using the second insulating layer as a mask, etching through the first insulating layer to extend the via opening, stopping at a surface of the semiconductor body, simultaneously etching the exposed portion of the first masking layer;

using the first and second masking layers as a mask, etching the second insulating layer through to the surface of the first insulating layer, simultaneously etching any exposed portion of any protective cap layer on the surface of the semiconductor body, and exposing the top surface of a metal conductor or circuit element at the bottom of the via opening;

depositing upon the semiconductor body a layer of metal conductor such as to contact the top surface of any underlying metal conductor or circuit element, to fill the previously opened via opening, to fill the previously defined opening in the second insulating layer, and overfilling said opening above the level of the top surface of the second masking level; and

planarizing the top surface of the semiconductor body so as to remove all metal conductor material above the top surface of the first masking layer and to remove the second masking layer.

2. The method of claim 1 wherein the first dielectric material is of a material having relatively high hardness, high moduli of elasticity, high thermal conductivity, and low coefficient of thermal expansion as compared to the corresponding characteristics of the second insulating layer.

3. The method of claim 1 wherein the second dielectric material is of a material having lower a dielectric constant than said first dielectric material.

4. The method of claim 1 wherein the first dielectric material is silicon dioxide.

5. The method of claim 1 wherein the second dielectric material is chosen from the class of materials known as organic dielectrics or polymers.

6. The method of claim 1 wherein the second dielectric material is chosen from one of a class of materials consisting

of low-k CVD silicon oxide and a group of mixtures of silicon, oxygen, carbon, fluorine, and hydrogen.

7. The method of claim 1 wherein the first masking material is silicon nitride.

8. The method of claim 1 wherein the second masking material is a metal.

9. The method of claim 1 wherein the second masking material is tungsten.

10. The method of claim 1 wherein the first insulating layer and the exposed portion of the first masking layer are etched in separate, but sequential, operations.

11. The method of claim 1 wherein the second insulating layer and the exposed portion of any protective cap layer on the surface of the semiconductor body are etched in separate, but sequential, operations.

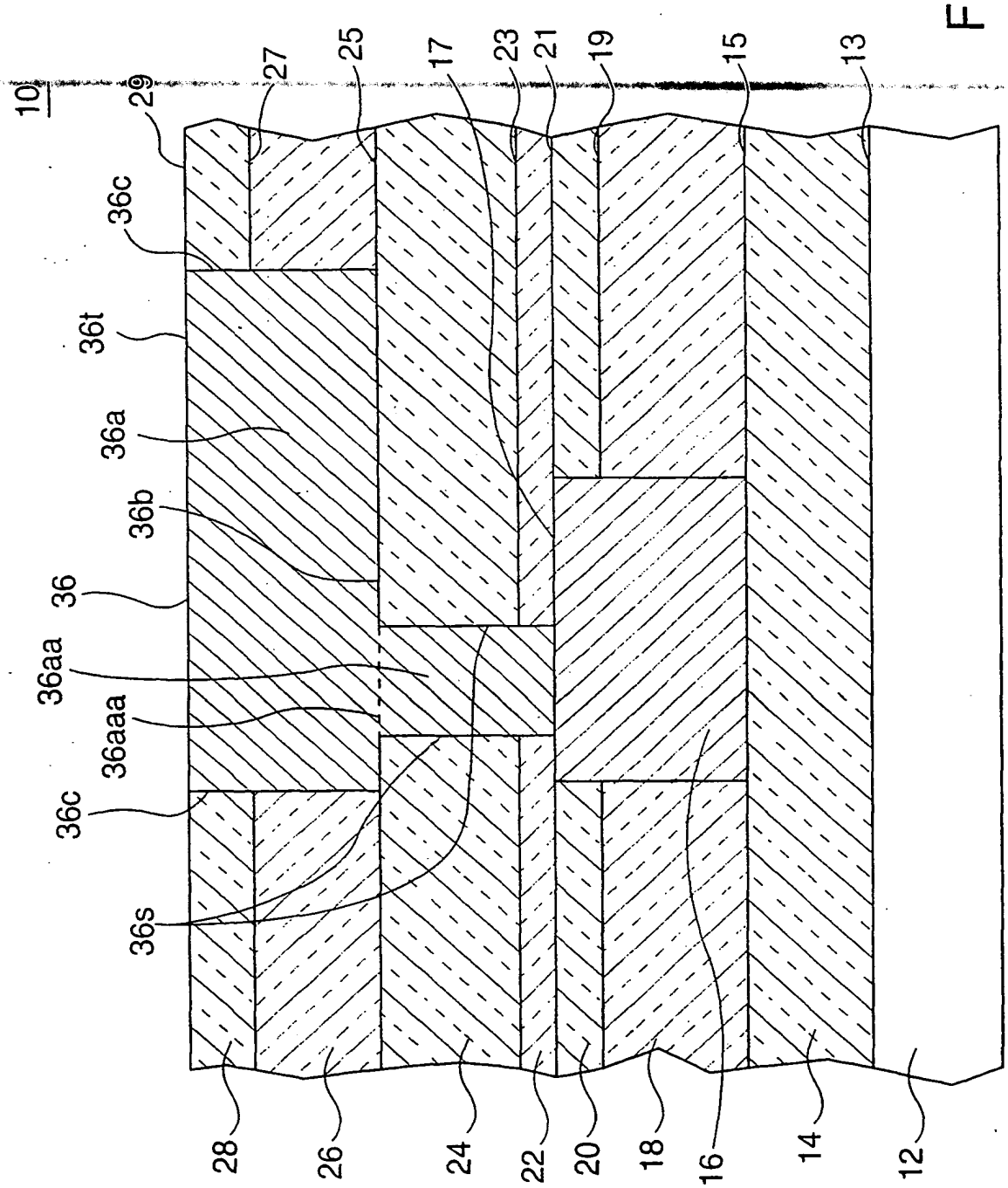

10
29
27
25
17
23
21
19
15
13
36c
36t
36a
36b
36
36aa
36aaa
36c
36s
28
26
24
22
20
18
16
14
12

FIG. 1

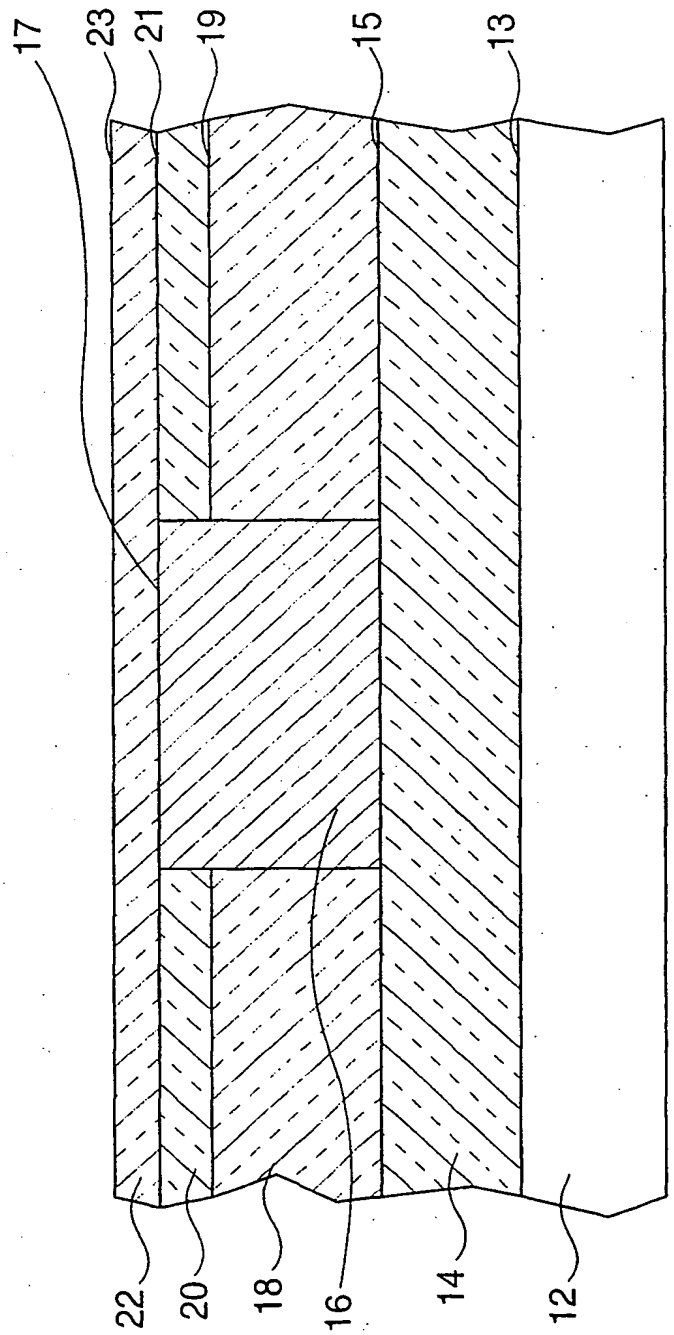


FIG. 2

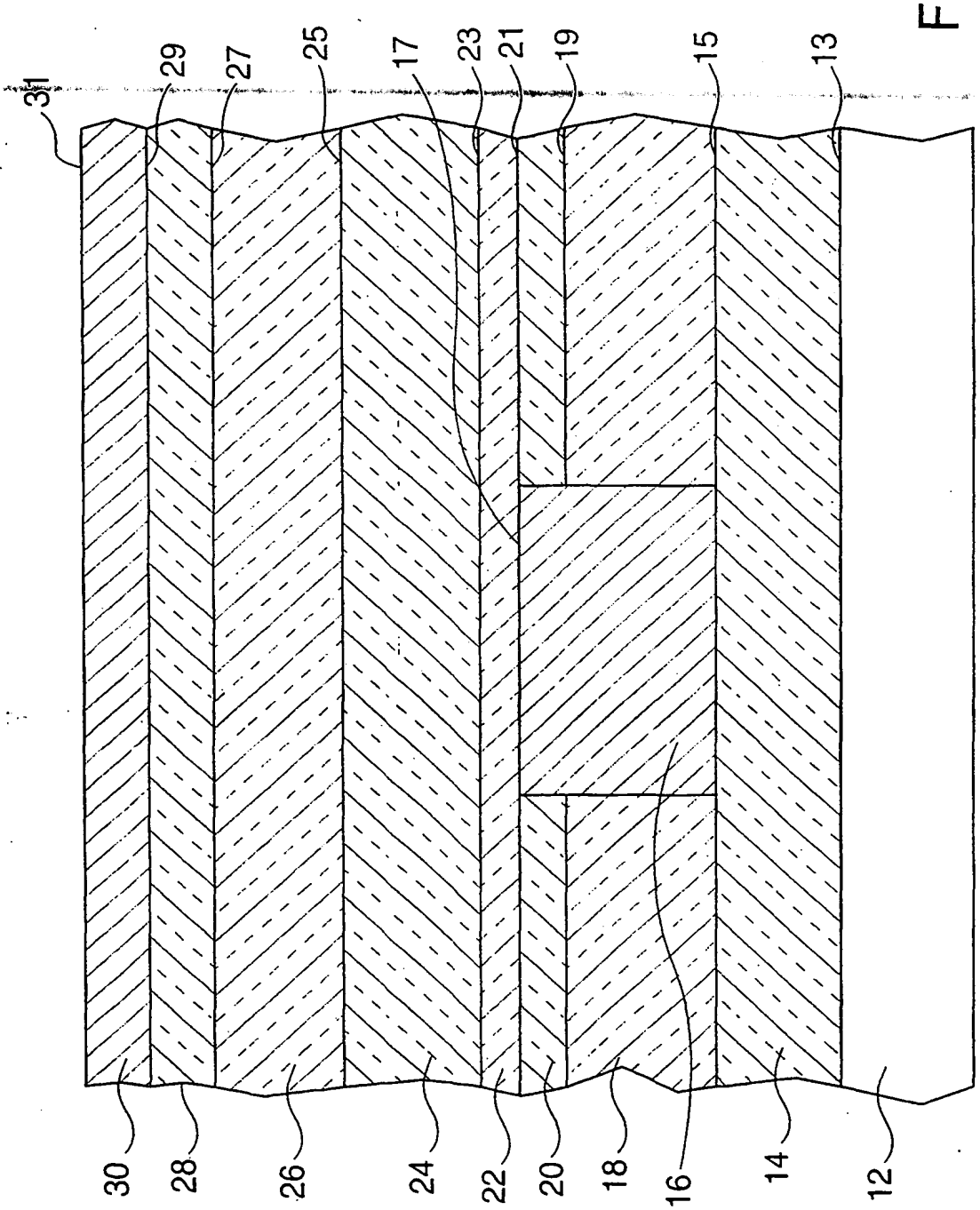


FIG. 3

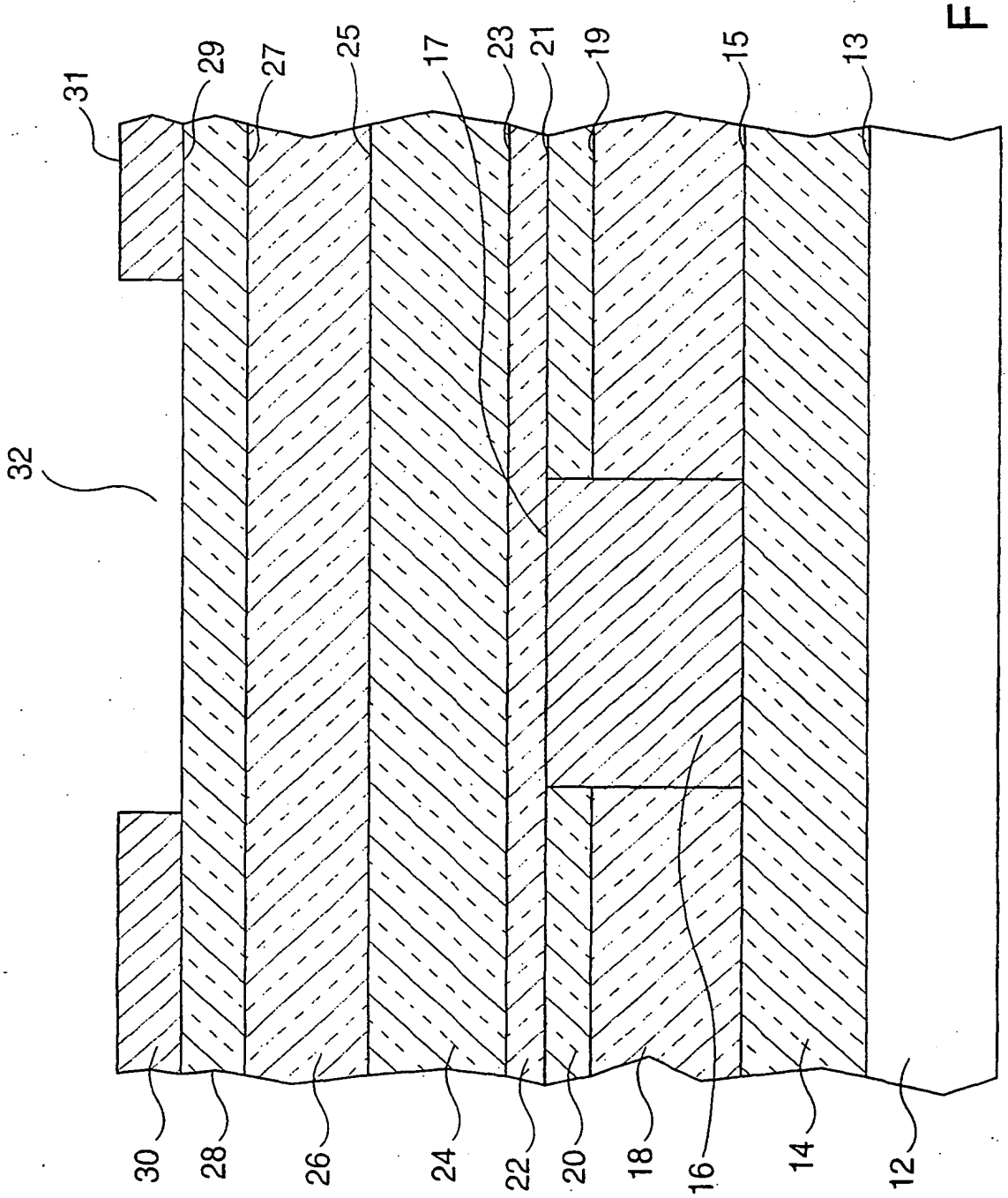


FIG. 4

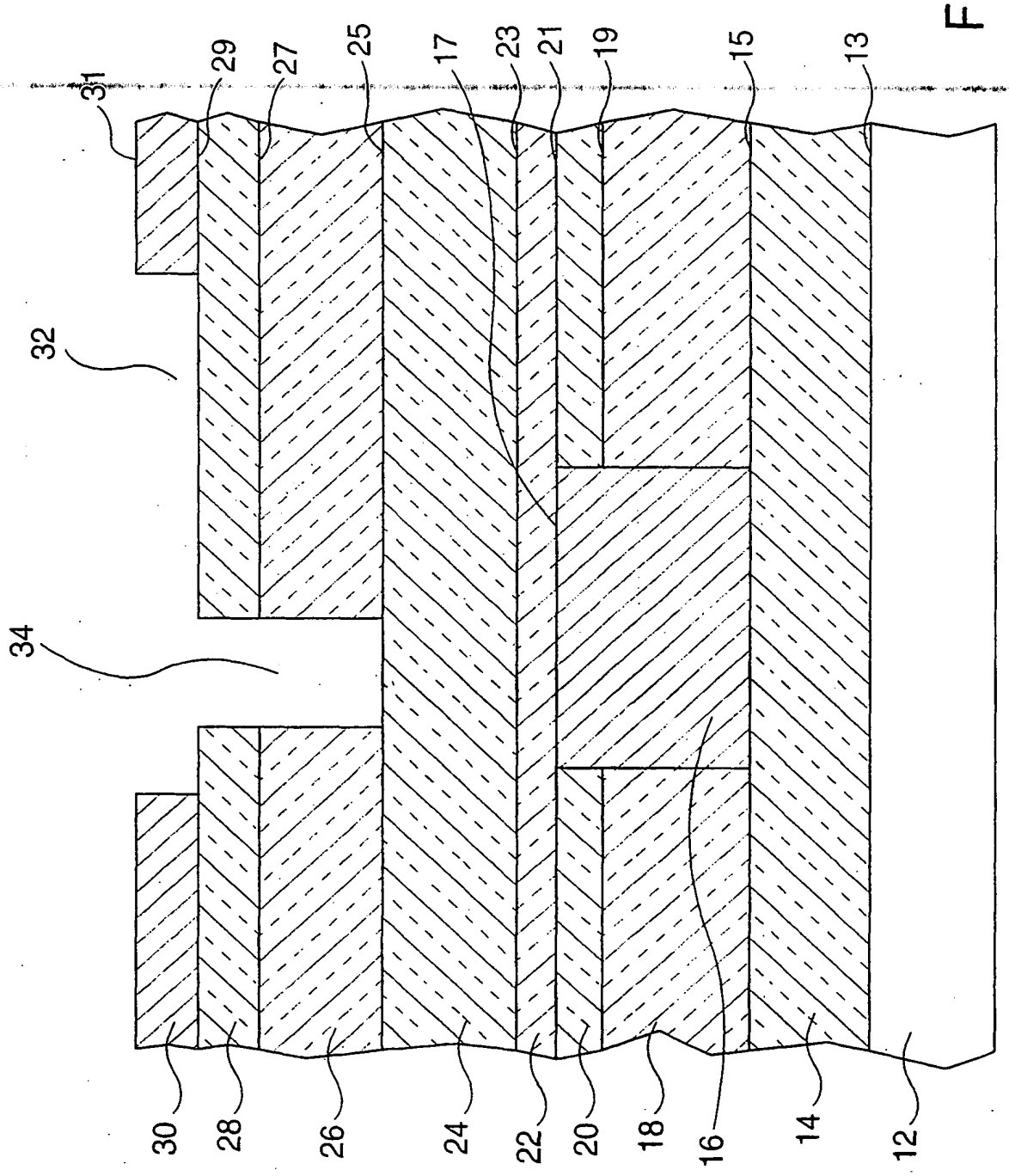


FIG. 5

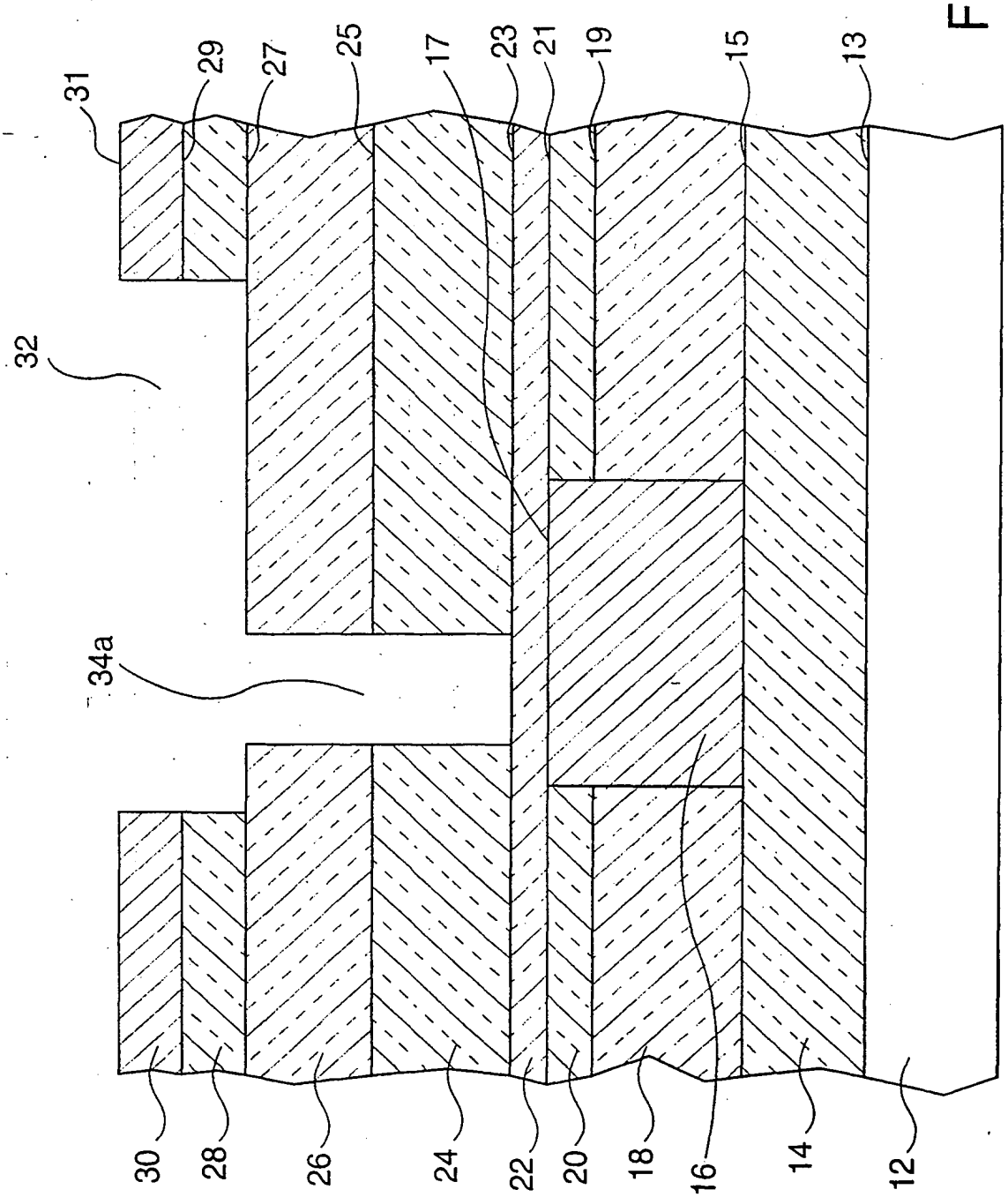


FIG. 6

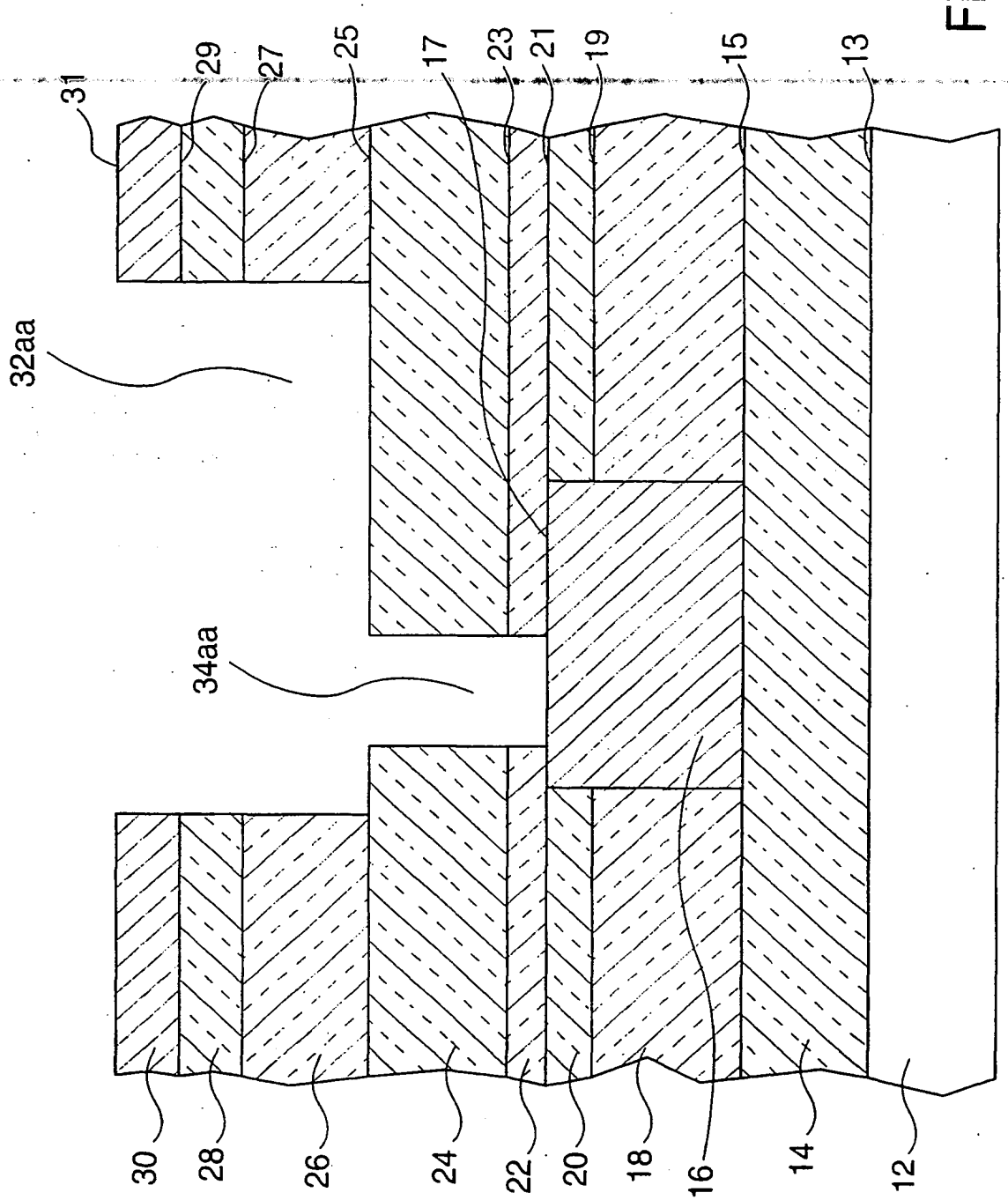


FIG. 7

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 December 2001 (27.12.2001)

PCT

(10) International Publication Number
WO 01/99184 A3

(51) International Patent Classification[7]: H01L 21/768, 23/532

(21) International Application Number: PCT/US01/19881

(22) International Filing Date: 21 June 2001 (21.06.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/598,780 21 June 2000 (21.06.2000) US

(71) Applicant: INFINEON TECHNOLOGIES NORTH AMERICA CORP. [US/US]; 1730 North First Street, San Jose, CA 95112-4508 (US).

(72) Inventors: STETTER, Michael; 12-7 Loudon Dr., Fishkill, NY 12524 (US). KALTALIOGLU, Erdem; 16F Winthrop Road, Wappingers Falls, NY 12590 (US). COWLEY, Andy; 8 Summerlin Court, Wappingers Falls, NY 12590 (US).

(74) Agents: BRADEN, Stanton, C. et al.; Siemens Corporation - Intellectual Property Dept., 186 Wood Ave. South, Iselin, NJ 08830 (US).

(81) Designated States (national): JP, KR.

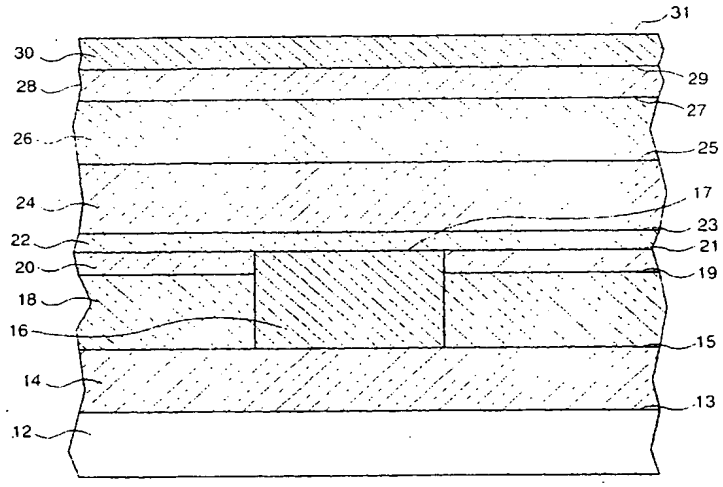
(84) Designated States (regional): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:
— with international search report

(88) Date of publication of the international search report:
27 June 2002

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: DUAL DAMASCENE PROCESS UTILIZING A LOW-K DUAL DIELECTRIC



(57) Abstract: A method of fabricating an integrated circuit with a dual dielectric structure and utilizes a dual damascene process to fabricate metal interconnection layers. The dual dielectric structure consists of a first insulating layer (24) of conventional dielectric material, and a second insulating layer (26) of a second dielectric material with a low dielectric constant (low-k dielectric material). The first dielectric material is used in regions of the integrated circuit where the superior mechanical properties of conventional dielectric materials will result in maintaining the reliability and mechanical properties of the integrated circuit. The second dielectric material is used in regions of the integrated circuit where the low dielectric constant will result in improved speed of the integrated circuit and reduced electrical coupling between conductors in the integrated circuit. The fabrication of the dual dielectric structure is integrated with a dual damascene metallization process.

WO 01/99184 A3

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/19881

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/768 H01L23/532

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	EP 0 945 900 A (MATSUSHITA ELECTRIC IND CO LTD) 29 September 1999 (1999-09-29) column 20, line 20 -column 25, line 28; figures 15-17	1-6,8,11 7
A	US 5 821 169 A (PENG CHIEN-HSIUNG ET AL) 13 October 1998 (1998-10-13) column 8, line 20 - line 26 column 10, line 20 -column 11, line 30; figures 19-27	1,7-10
P,X	US 2001/002331 A1 (MIYATA KOJI) 31 May 2001 (2001-05-31) paragraph '0065! - paragraph '0078!; figure 2	1-5,8,9

☐ Further documents are listed in the continuation of box C

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 January 2002	30/01/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Micke, K

1

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 01/19881

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0945900 A	29-09-1999	EP 0945900 A1	29-09-1999
		JP 3062491 B2	10-07-2000
		JP 2000003913 A	07-01-2000
		JP 3078811 B2	21-08-2000
		JP 2000294643 A	20-10-2000
		JP 3078812 B2	21-08-2000
		JP 2000294644 A	20-10-2000
		US 6197696 B1	06-03-2001
		US 2001001739 A1	24-05-2001
US 5821169 A	13-10-1998	JP 10172963 A	26-06-1998
US 2001002331 A1	31-05-2001	JP 2001156170 A	08-06-2001